

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Previously Presented) A semiconductor structure, comprising:
  - a substrate;
  - a patterned oxide layer disposed over the substrate;
  - a layer of undoped silicate glass disposed over the patterned oxide layer;
  - a layer of borophosphorous silicate glass over the layer of undoped silicate glass;
  - a planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a first portion of the layer of the borophosphorous silicate glass, and not overlaying at least a second portion of the borophosphorous silicate glass layer, the second portion separated by a distance from the first portion; and
    - a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least the second portion of the borophosphorous silicate glass region, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and said layer of plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack.
2. (Previously Presented) The structure of claim 1 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2,000 and 8,000 angstroms.
3. (Previously Presented) The structure of claim 1 wherein the second layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. (Previously Presented) The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than 15,000 angstroms.

5. (Canceled)

6. (Currently Amended) An integrated circuit, comprising:  
a substrate;  
a first dielectric layer disposed on the substrate;  
a layer of undoped silicate glass disposed on the dielectric layer;  
an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said unplanar layer having an uppermost surface;  
a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and  
a second dielectric layer disposed on the planar dielectric layer and the uppermost surface of said unplanar layer of borophosphorous silicate glass, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and said second dielectric layer together composing a pre-metal dielectric stack.

7. (Original) The integrated circuit of claim 6 wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

8. (Canceled)

9. (Previously Presented) The integrated circuit of claim 6 wherein the second dielectric layer is tetraethyl orthosilicate

10. (Previously Presented) The integrated circuit of claim 6 wherein the second dielectric layer is plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

11-19. (Canceled)

20. (Previously Presented) A semiconductor device sub-structure, comprising:

a substrate;

an oxide layer disposed over the substrate in a pattern having a physical contour of at least one or more recessed portions and at least one or more extended portions;

a layer of undoped silicate glass disposed over the patterned oxide layer and having a physical contour of recessed and extended portions corresponding to the physical contour of the oxide layer;

a layer of doped silicate glass over the layer of undoped silicate glass and having a physical contour of recessed and extended portions corresponding to the physical contour of the layer of undoped silicate glass;

a first substantially planar layer of dielectric material covering at least one or more of the recessed portions of the layer of the doped silicate glass, and exposing at least one or more of the extended portions of the layer of the doped silicate glass layer; and

a second layer of dielectric material covering the first substantially planar layer of dielectric material and being in direct contact with the at least one or more extended portions of the layer of the doped silicate glass layer.

21. (Canceled)

22. (Previously Presented) The device of claim 20 wherein the layer of doped silicate glass is a layer of borophosphorous silicate glass.

23. (Previously Presented) The device of claim 22 wherein the first layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

24. (Previously Presented) The device of claim 23 wherein the second layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

25. (Previously Presented) The device of claim 24 wherein the second layer of dielectric material is substantially planar.

26. (Previously Presented) The device of claim 25 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2,000 and 8,000 angstroms.

27. (Previously Presented) The device of claim 26 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than 15,000 angstroms.

28. (Previously Presented) A semiconductor structure, comprising:  
a substrate;  
a patterned oxide layer disposed over the substrate;  
a layer of undoped silicate glass disposed over the patterned oxide layer;  
a layer of borophosphorous silicate glass over the layer of undoped silicate glass, said layer of borophosphorous silicate glass having an upper surface having a highest surface region and a lowest surface region;

a planarized layer of plasma-enhanced tetraethyl orthosilicate disposed on said layer of borophosphorous silicate glass said planarized layer having a thickness less than or approximately equal to a difference in the highest surface region and the lowest surface region of the BPSG layer; and

a layer of plasma-enhanced tetraethyl orthosilicate overlaying and being in contact with the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with the highest surface region of the borophosphorous silicate glass region, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and said layer of plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack.